Design and Licensing of the NuScale SMR I&C Systems

HIPS platform was extremely successful. A purpose-built prototype of the HIPS platform was developed and manufactured by Ultra Electronics to demonstrate the functionality of the main HIPS modules and provide demonstration and proof-ofconcept that the key design requirements of the HIPS platform can be met.

In a conventional PWR, the primary system consists of a reactor pressure vessel, pressurizer, steam generators, reactor coolant pumps, and the connecting piping. Performing flow measurements in a conventional PWR with forced circulation and piping is straightforward and well established. In contrast, the novel and unique design of the NuScale Power Module has no primary system loop piping or forced circulation; the reactor is cooled by natural circulation.

To demonstrate the feasibility of measuring reactor coolant flow measurements inside the NuScale reactor pressure vessel, a full-scale (radially) high-fidelity prototype reactor pressure vessel model was designed and manufactured by Cameron and Alden Labs to perform flow measurement tests for the flow regions of interest. Computational fluid dynamics analysis and extensive testing were performed to demonstrate proof-of-concept and gain important insights and understanding of flow measurements in low-flow conditions



Fig. 5. NuScale safety display and indication system

that exist in the NuScale SMR. The fully assembled reactor pressure vessel flow model prototype is shown in Fig. 4.

Another important FOAK development effort was completed for the safety display and indication system (SDIS)[2]. The SDIS provides plant operators with information and data to ensure that the plant is operating within the limits defined by the plant safety analyses, and it also provides accurate, complete, and timely information to support long-term post-accident monitoring. The application of FPGA technology to the SDIS design was selected to ensure that the key design requirements would be met and to leverage the ongoing FPGA work associated with the HIPS platform. *Continued* 

